What is claimed is:

1. A ferroelectric random access memory (FRAM) device comprising:

a lower electrode;

a lower seed layer formed on the lower electrode;

a ferroelectric layer formed on the lower seed layer;

an upper seed layer formed on the ferroelectric layer; and

an upper electrode formed on the upper seed layer.

2. The FRAM device according to claim 1, wherein the ferroelectric layer is a PZT layer.

3. The FRAM device according to claim 1, wherein the upper and lower seed layers make characteristics of an upper interface and a lower interface of the ferroelectric match each other.

4. The FRAM device according to claim 1, wherein the upper and lower seed layers are composed of a material having a crystallization temperature lower than that of a material of the ferroelectric layer.

5. The FRAM device according to claim 1, wherein the upper and lower seed layers are composed of a ferroelectric material having a lattice constant similar to that of

a material of the ferroelectric layer.

6. The FRAM device according to claim 2, wherein the upper and lower seed layers are composed of $PbTiO_3$, TiO_2 or PZT having at least one of a higher Pb content and a higher Ti composition ratio than the PZT of the ferroelectric layer.

7. The FRAM device according to claim 1, wherein the upper and lower electrodes include a Pt-group metal layer, a conductive oxide layer or a dual layer of the Pt-group metal layer and the conductive oxide layer.

8. The FRAM device according to claim 1, further comprising:

a switching element electrically connected to the lower electrode.

9. The FRAM device according to claim 1, further comprising:

a gate insulating layer under the lower electrode;

a semiconductor substrate under the gate insulating layer; and

source and drain regions in a portion of the semiconductor substrate adjacent to a periphery of the gate insulating layer.

10. The FRAM device according to claim 6, wherein the upper and lower electrodes include of a Pt-group metal layer, a conductive oxide layer or a dual layer of

the Pt-group metal layer and the conductive oxide layer.

11. The FRAM device according to claim 1, wherein the upper and lower electrodes have the same structure.

12. The FRAM device according to claim 1, wherein the upper and lower seed layers are composed of the same material.

13. A method for fabricating a ferroelectric random access memory (FRAM) device comprising:

a) forming a lower electrode;

b) forming a lower seed layer on the lower electrode;

c) forming a ferroelectric layer on the lower seed layer;

d) forming an upper seed layer on the ferroelectric layer;

e) annealing a structure resulting from a)-d), including making characteristics of a lower face and an upper face of the ferroelectric layer be the same and completing a stable perovskite crystal structure of the ferroelectric layer; and

f) forming an upper electrode on the upper seed layer.

14. The method according to claim 13, wherein forming a ferroelectric layer comprises forming a PZT ferroelectric layer on the lower seed layer.

15. The method according to claim 13, wherein the forming the upper and lower seed layers includes using a material having a crystallization temperature lower than that of a material for forming the ferroelectric layer.

16. The method according to claim 13, wherein the forming the upper and lower seed layers includes using a ferroelectric material having a lattice constant similar to that of a material for forming the ferroelectric layer.

17. The method according to claim 14, wherein the forming the upper and lower seed layers includes using $PbTiO_3$, TiO_2 or PZT having at least one of a higher Pb content and a higher Ti composition ratio than a PZT to be used to form the ferroelectric layer.

18. The method according to claim 13, wherein the forming the lower electrode and the upper electrode includes using a Pt-group metal layer, a conductive oxide layer or a dual layer of the Pt-group metal layer and the conductive oxide layer.

19. The method according to claim 13, further comprising, prior to the forming the lower electrode, forming a switching element to be electrically connected to the lower electrode.

20. The method according to claim 13, further comprising:

before the forming the lower electrode

providing a semiconductor substrate; and

forming a gate insulating layer on the semiconductor substrate, and

after the forming the upper electrode

forming source and drain regions in a portion of the semiconductor substrate adjacent to a periphery of the gate insulating layer.